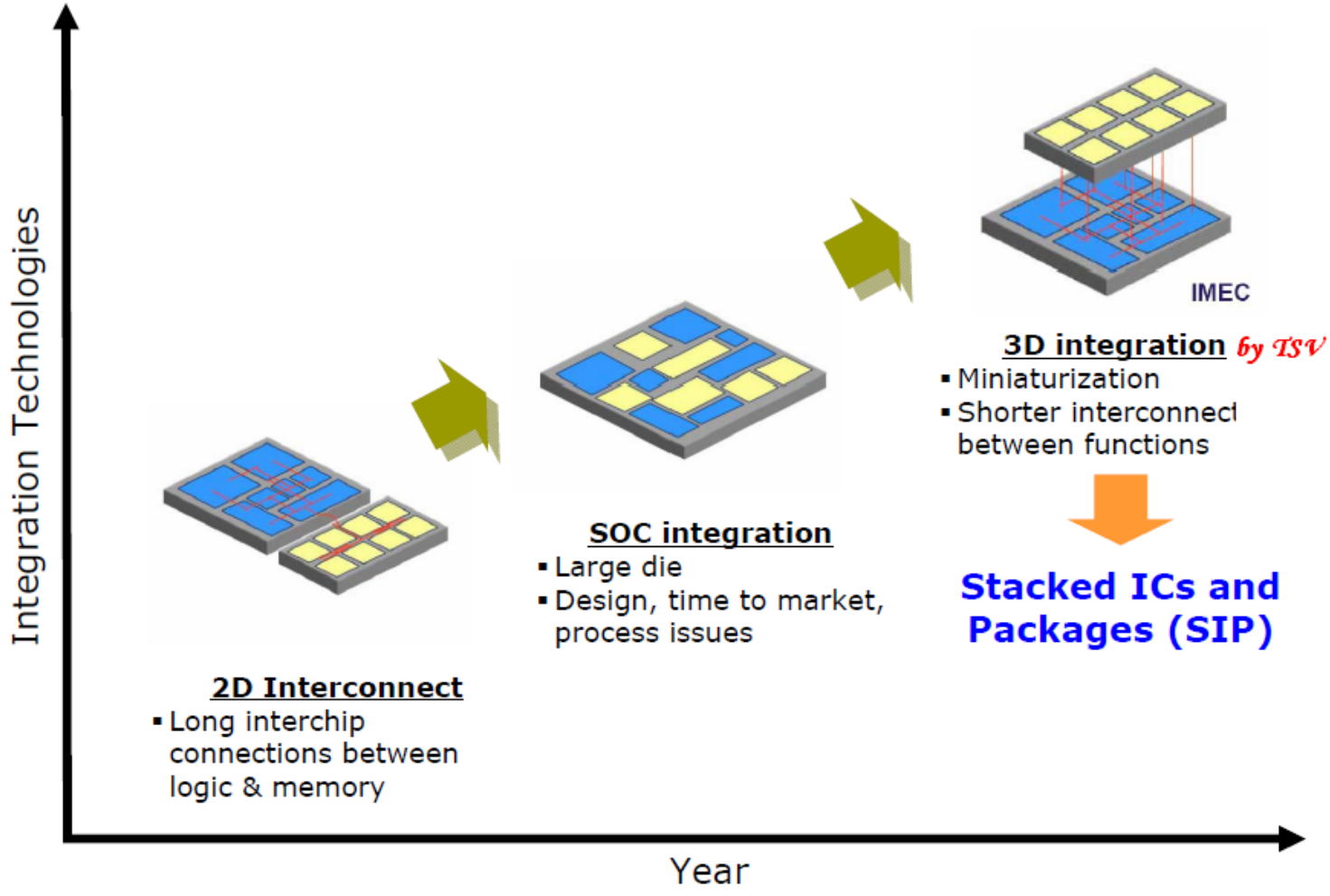
Fabrication of Through Silicon Via (TSV) in Stacked ICs and Packages (SIP)

Through Silicon Via (TSV)

- A through-via hole drilled in silicon and filled with conductor material to form vertical electrical interconnections.
- Drivers:
  - Size reduction
  - Solving the "interconnect bottleneck" of traditional interconnect technologies
  - Heterogeneous integration of different technologies
  - Higher electrical performance

System Integration



Figures provided in lecture "Introduction to System-In-Package (SIP)", Baik Woo Lee, ECE6776, 8/28/2008

TSV vs. Wire Bonding

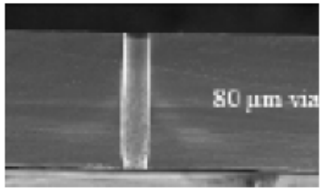
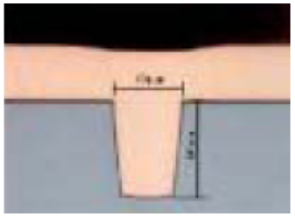
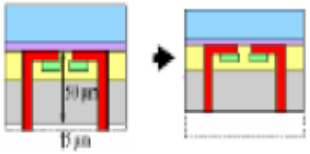
Characteristics	TSV	Wire Bonding
Interconnect arrangement	Can be area array or peripheral	Only peripheral interconnect
Interconnect length	Shorter	Much longer
Electrical parasitic	Much lower	Higher
I/O density	Potentially high	Lower
Reliability	Higher	Less reliable
Processing	IC fabrication process	Packaging Process

Table provided in book "Introduction to System-On-Package (SOP)", Rao R. Tummala, Madhavan Swaminathan, Pg. 123

TSV Fabrication Steps

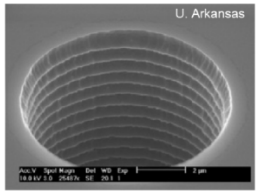
- Via drilling
- Via filling
- Chip/Wafer bonding
- Thinning

Basic TSV Enabling Technologies

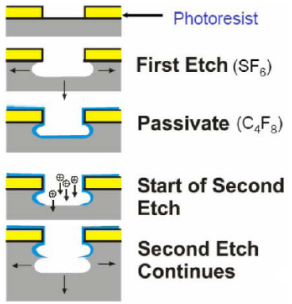
Via Formation	Via Filling	Chip/Wafer Bonding		Thinning
				
		C2C/C2W	W2W	
Technologies				
▪ Wet etching ▪ Laser drilling ▪ Bosch DRIE ▪ Cryogenic DRIE	▪ Electroplating ▪ CVD ▪ Photolithography	▪ Adhesive bonding ▪ Metal-Metal bonding ▪ Chip alignment	▪ Adhesive bonding ▪ Metal-Metal bonding ▪ Wafer alignment	▪ Grinding ▪ CMP ▪ Wet etching ▪ Plasma etching
Equipments				
▪ Laser or DRIE DRIE ▪ Spin Coater ▪ Mask aligner or stepper	▪ Mask deposition system ▪ Coater ▪ Mask aligner or stepper	▪ Device bonder ▪ Device aligner	▪ Waver bonder ▪ Wafer aligner	▪ Thinning equipment ▪ Temporary bonder

Figures provided in lecture "Introduction to System-In-Package (SIP)", Baik Woo Lee, ECE6776, 8/28/2008

Via Drilling

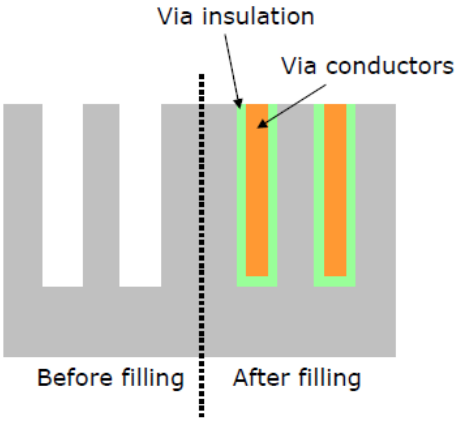


- Bosch-type deep reactive ion etching (DRIE)
  - Alternating passivation and etching – makes smooth straight side walls
- Cryogenic DRIE
  - Similar to ordinary DRIE but at cryogenic temperatures (-110 °C)
  - Lowers ion mobility – very little side etching
- Wet etching
  - Isotropic and anisotropic processes
- Laser drilling
  - Creates silicon "splashes" due to "melting" – should be at least 2um away from active devices
  - Via sidewall slope from 1.3° to 1.6°



Figures provided in lecture "Introduction to System-In-Package (SIP)", Baik Woo Lee, ECE6776, 8/28/2008

Via Filling



- Insulating films
  - Thermal
  - Plasma-enhanced chemical vapor deposition (PECVD)
  - low pressure chemical vapor deposition (LPCVD) nitrides
- Metallization
  - Done using sputtering and laser assisted chemical vapor deposition (CVD)
  - Materials like Cu, W, and polysilicon are used
  - Cu – good electrical conductivity, bad CTE mismatch (bad for deep TSVs)

Figures provided in lecture "Introduction to System-In-Package (SIP)", Baik Woo Lee, ECE6776, 8/28/2008

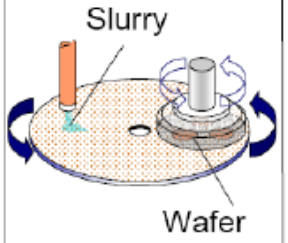
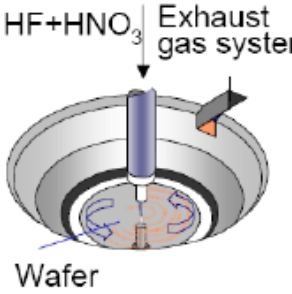
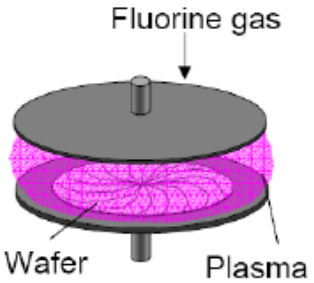
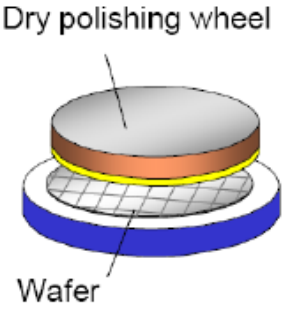
Chip/Wafer Bonding

- Oxide bonding
  - Coated with low temp oxides (LTO) and heat at high temp – covalent bonds at interface
  - Compatible for BEOL wafer processing
- Metal-metal bonding
  - Cu-Sn eutectic bond – bonding through diffusion, reliability enhanced with resin encapsulation
  - Cu-Cu direct bond – more reliable, postbond annealing done to induce diffusion, grain growth and crystallization
- Polymer bonding
  - Thermoplastic and thermosetting polymers that are bonded using vacuum pressure and curing

Thinning and Polishing

- Grinding
  - Oxidized metal abrasive in polishing
- Chemical mechanical polishing (CMP)
  - Uses chemical slurry to thin wafer
- Wet etching
  - HF+HNO3 solution to etch wafer
- Plasma etching
  - Uses fluorine gas to etch wafer

Thinning and Polishing

Process	CMP (Chemical Mechanical polishing)	Wet Etching	Dry Etching (Plasma)	Dry Polishing
				
Reacting Substance	Slurry	$HF+HNO_3$	Fluorine gas	Oxidized metal abrasive
Processing rate	1 μm/min	> 10 μm/min	2 μm/min	1 μm/min
Productivity	Good	Excellent	Good	Good
Die strength	Good	Good	Good	Good
Environmental condition	Slurry management required	Generates NOx	SF6	Excellent
*Running cost	Acceptable	Acceptable	Acceptable	Excellent

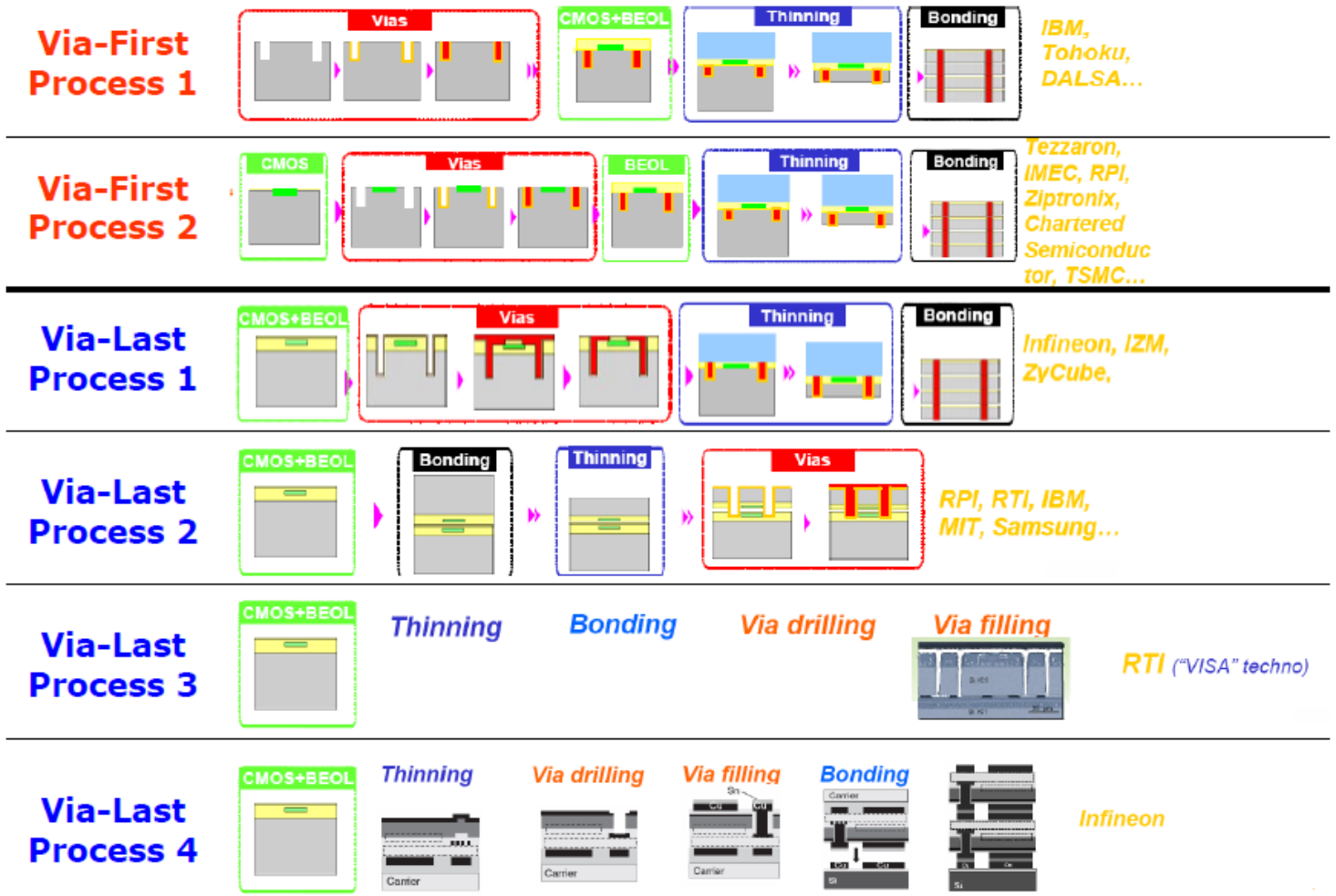
Figures provided in lecture "Introduction to System-In-Package (SIP)", Baik Woo Lee, ECE6776, 8/28/2008

3D Integration

Step No.	Via-First	Via-Last
1	TSV drilling	BEOL wiring development
2	Dielectric deposition	Wafer mounting and thinning
3	Passivation and via filling	TSV formation from back of wafer
4	BEOL wiring development	Dielectric deposition
5	Wafer thinning to make contact with TSV	Passivation and via filling
6	Interconnect development on back of wafer	Interconnect development on back of wafer

Table provided in book "Introduction to System-On-Package (SOP)", Rao R. Tummala, Madhavan Swaminathan, Pg. 135

Various Integration Approach



Figures provided in lecture "Introduction to System-In-Package (SIP)", Baik Woo Lee, ECE6776, 8/28/2008